IIIT BANGALORE

No: MIIT/54/18 Date: 20th March 2018

Amendment-I

Subject: Supply, Installation, testing and commissioning and on-site support of setting up of VLSI Laboratory.

International Institute of Information Technology (IIIT) Bangalore on be-half of Ministry of External Affairs (MEA) invites sealed tenders from eligible bidders for supply, installation, testing & commissioning and on-site support for setting up of **VLSI Laboratory** for Myanmar Institute of Information and Technology (MIIT) at Mandalay in Myanmar on turnkey basis vide IIIT-B MIIT/52/18 dated 23rd February 2018

2. The following amendments are made in the above mentioned tender document.

Name of Work	***EMD***	***Last date bid submission***	***Date opening of bids***
Supply, Installation, testing & commissioning and on-site support of VLSI Laboratory	**Rs 4.1 Lac**	**06th April 2018 at 1300 hours**	**06th April 2018 at 1400 hours**

3. The clarifications/responses to the queries listed in the pre-bid meeting are mentioned Annexure I of this amendment.

4.All other terms and conditions remain same.

Registrar IIIT-Bangalore

International Institute of Information Technology
(MIIT Mentoring Cell)

20th March 2018

Tender Reference:- MIIT/52/18 for supply, installation, testing & commissioning and onsite support for installation and setting up of VLSI Laboratory for Myanmar Institute of Information and Technology (MIIT) at Mandalay in Myanmar on turnkey basis.

Following clarifications are issued in response to the queries received from Prospective bidders:

Sl no	Tender Queries	Clause as published in the tender	Remarks/sub mission/Justifi cation	Clarifications/Corrigend a/Amendment
01	Section 1, Clause 2 g	Relevant ISO certificate in IT Infrastructure.	Please allow relevant ISO certificate in Laboratory / Communication and Testing & Measurement equipment's / IT Infrastructure	The change is accepted
02	Section 1, Clause 2 i	The copy of Supply Orders/ Contracts/ Agreements issued by/ signed with Government of India (Ministry/ Department/ Undertaking/ PSU/ Educational Institutions such as IIT's, NIT's, or other such Central Universities/Banking sector/lT-SEZs/Technology parks/ Stock/Commodity exchanges and reputed private organizations including educational institutions in India) for similar work, executed by the bidders in last five years ending December 31st 2017. The bidder should also enclose the completion certificate duly issued by the end user. The bidder should have completed at least ONE similar work not less than Rs. 1.64 Cr OR TWO similar works not less than Rs. 1.02 Cr OR THREE similar works not less than 82 Lakh. The similar work means supply & installation of all/ most of the items mentioned in	Please allow the similar work should mean setup of any scientific/testing and measurement / forensic/ securedmessaging/communic ation lab/ TV studio lab/IT Lab. This will help in bringing more bidders participation.	The tender conditions, ask for experience in similar work undertaken by the bidder. Hence, scientific lab/communication lab is also part of similar work already outlined in the tender terms and conditions

		this tender document in a single project on turn-key basis in India/abroad.		
03	Section 2, Clause 1	The delivery and installation at site(s) must be completed within 60 days from the date of placement of supply order by IIIT Bangalore. All the necessary spare parts and tools required for installation and commissioning of the tendered item will have to be supplied along with the tendered items. The custom clearance of the equipment would be facilitated by Indian Mission in Myanmar. The tendered equipment will be exempted from payment of Myanmar custom duties. It is mandatory for the bidders who respond to this bid to meet these expectations as time is the essence of this contract and is tightly linked to completing the project within the available time frame.	Please allow minimum 160 days for supply, installation, testing and commissioning of VLSI lab at MIIT, Mandalay, Myanmar instead of 60 days as sourcing of such items is time consuming including dispatch & clearance formalities.	The change is partially accepted. The revised delivery and installation is now 90 days
04	Section 3, Clause 7	i. IIIT Bangalore shall release 5% of the payment upon purchase order subject to receipt of the performance bank guarantee as outlined in clause 8 below. ii. IIIT Bangalore shall release 35% of the payment upon dispatch of the tendered items subject to submission of original shipping documents and BL. iii. IIIT Bangalore shall release 30% of the payment upon delivery of the tendered items at MIIT subject to satisfactory certificate of receipt by Embassy of India, Yangon and/or MIIT/IIIT-Bangalore. iv. Payment of 30% of the purchase order value will be made after physical verification by a Project	Please allow 70% payment on dispatch against submission of original invoice packing list, copy of bill lading / AWB and copy of insurance & the balance eof 30 % against installation, testing and commissioning duly signed by Embassy of India and /or MIIT/ or IIIT Bangalore.	The current payment terms are already in effect for the other tenders being administered for this project. **The change is not accepted.**

		Monitoring Committee (PMC). v. In case of foreign bidders who quoted in US $, letter of credit(LC) will be opened and payment would be released as per 7(i), 7(ii), 7(iii) and 7(iv).		
05	Section III, Clause 1, sub clause 1.2	2.Bidders should quote the prices in INR or in US $ and as per the format given in Price Schedule at Section – V of this document.	Kindly correct payment terms sub point –V and delete foreign bidder.	The change is not accepted.
06	Section 1, Clause g	Relevant ISO certificate in IT Infrastructure.	Please allow ISO Certificate in the IT Infrastructure, Test & measurement Equipment & Laboratory Infrastructure.	The query is answered in Sl no 1.
07	Section II, Clause 4.2	The bidder should also enclose the completion certificate duly issued by the end user. The bidder should have completed at least ONE similar work not less than Rs. 1.64 Cr OR TWO similar works not less than Rs. 1.02 Cr OR THREE similar works not less than 82 Lakh. The similar work means supply & installation of all/ most of the items mentioned in this tender document in a single project on turn-key basis in India/abroad.	Please allow past experience as setting up of any Technical IT lab / Education/ Scientific Research Laboratory as products desired are used for teaching / or use in Embedded IT Systems solution.	The query is answered in Sl no 2.
08	Section II, Clause 1	Delivery Period / Project Timelines: The delivery and installation at site(s) must be completed within 60 days from the date of placement of supply order by IIIT Bangalore.	Please allow more time for delivery & completion at site i.e. minimum 190 days from the date of placement of supply order by IIIT Bangalore.	The change is partially accepted. The revised delivery and installation is now 90 days
09	Section III, Clause 7	Payment Terms: Payments: i. IIIT Bangalore shall release 5% of the payment upon purchase order subject to receipt of the performance bank guarantee as outlined in clause 8 below. ii. IIIT Bangalore shall release 35% of the payment upon dispatch of the tendered items subject	Please change payment terms to market friendly for wider participation and competitive price. 90% payment against the submission of proof of Delivery and 10% balance payment of the purchase order value made after physical verification by a End	The current payment terms are already in effect for the other tenders being administered for this project. **The change is not accepted.**

		to submission of original shipping documents and BL. iii. IIIT Bangalore shall release 30% of the payment upon delivery of the tendered items at MIIT subject to satisfactory certificate of receipt by Embassy of India, Yangon and/or MIIT/IIIT-Bangalore. iv. Payment of 30% of the purchase order value will be made after physical verification by a Project Monitoring Committee (PMC). v. In case of foreign bidders who quoted in US $, letter of credit(LC) will be opened and payment would be released as per 7(i), 7(ii), 7(iii) and 7(iv).	user and submission of 10% Performance Bank Guarantee	
10	Warranty	All the items covered in the schedule of requirements, shall carry minimum 5 (five) years on site comprehensive warranty from the date of its installation & commissioning. The bidder must undertake to provide the installation and warranty service in Myanmar. The repairing/ rectification/ replacement/ configuration required, if any, must be done at site only. During the warranty, all complaints should be rectified within 7 days from the time of complaint. In case the rectification of fault involves replacement of some hardware the same should be carried out within 21 days from the date of intimation. Failure to do so would result in the invoking of the PBG. The PBG will be released by IIIT Bangalore only after the submission of satisfactory	Based on last few IIIT Bangalore tenders & corrigendum issued, our technical team had noticed the warranty desired, is 2 Years. However in this particular case the warranty desired is 5 years. Please clarifiy.	The warranty required is for 2 years.

		performance certificate issued by MIIT / Indian Mission & end-user after the completion of warranty period. The Purchaser reserves the right to reject any set of equipment found defective within 30 days after the date of acceptance of equipment. The cost towards replacement will have to be borne by the supplier.		
11	Section 1, clause g	Relevant ISO certificate in IT Infrastructure.	Kindly amend the relevant ISO certificate in IT infrastructure to relevant ISO in laboratory Infrastructure/IT infrastructure and measurement equipment as VLSI is part of all these infrastructure field's.	The query is answered in Sl no 1.
12	Section II, clause 4.2	The copy of Supply Orders/ Contracts/ Agreements issued by/ signed with Government of India (Ministry/ Department/ Undertaking/ PSU/ Educational Institutions such as IIT's, NIT's, or other such Central Universities/Banking sector/lT-SEZs/Technology parks/ Stock/Commodity exchanges and reputed private organizations including educational institutions in India) for similar work, executed by the bidders in last five years ending December 31st 2017. The bidder Tender Document for Supply, Installation, Testing,Commissioning(SIT C) and onsite support for VLSI Laboratory of MllT project, Mandalay, Myanmar 8 of 31 should also enclose the completion certificate duly issued by the end user. The bidder should have completed at least ONE similar work not less than Rs. 1.64 Cr OR TWO similar works not less than Rs. 1.02 Cr OR THREE similar works	Similar work should mean setup of any scientific /ICT or IT lab instead of lab with similar items. We request that this definition should be changed wherever its appearing in the tender document. Also such VLSI FPGA board /products are not sold separately in banking sector or stock markets or commodity exchange. We therefore request you to delete the experience required from such sector banking , stock or commodity exchange sector since such products are part of scientific laboratory /ICT or IT (Information Technology) labs	The query is answered In Sl no 2.

		not less than 82 Lakh. The similar work means supply & installation of all/ most of the items mentioned in this tender document in a single project on turn-key basis in India/abroad.		
13	Section II, Clause 1	The delivery and installation at site(s) must be completed within 60 days from the date of placement of supply order by IIIT Bangalore. All the necessary spare parts and tools required for installation and commissioning of the tendered item will have to be supplied along with the tendered items. The custom clearance of the equipment would be facilitated by Indian Mission in Myanmar. The tendered equipment will be exempted from payment of Myanmar custom duties. It is mandatory for the bidders who respond to this bid to meet these expectations as time is the essence of this contract and is tightly linked to completing the project within the available time frame.	Please extend the period of delivery and installation at site(s) from 60 days to 150 days from the date of placement of supply order from IIIT Bangalore as these products are not available on shelf in market. Moreover this would require more packing custom clearance in dispatch country and thereafter custom clearance process in host country. Time frame of 60 days is too less for delivery, installation and commissioning at site.	The change is partially accepted. The revised delivery and installation is now 90 days
14	Section III, Clause 6	All the items covered in the schedule of requirements, shall carry minimum 5 (five) years on site comprehensive warranty from the date of its installation & commissioning.	Kindly restrict warranty 3 years for the items required in this tender as the support may not be available beyond 2 years such products get technological advance on fast track mode.	The query is already answered in S.No 10 above.
15	Section III, Clause 7	i. IIIT Bangalore shall release 5% of the payment upon purchase order subject to receipt of the performance bank guarantee as outlined in clause 8 below. ii. IIIT Bangalore shall release 35% of the payment upon dispatch of the tendered items subject to submission of original shipping documents and BL. iii. IIIT Bangalore shall release	Request to change the payment terms as following. 1. IIIT Bangalore shall release 5% of the payment upon purchase order subject to receipt of the performance bank guarantee as outlined in clause 8 below. 2. IIIT Bangalore shall release 75% of the payment upon dispatch of the tendered items subject to submission	The current payment terms are already in effect for the other tenders being administered for this project. **The change is not accepted.**

		30% of the payment upon delivery of the tendered items at MIIT subject to satisfactory certificate of receipt by Embassy of India, Yangon and/or MIIT/IIIT-Bangalore. iv. Payment of 30% of the purchase order value will be made after physical verification by a Project Monitoring Committee (PMC). v. In case of foreign bidders who quoted in US $, letter of credit(LC) will be opened and payment would be released as per 7(i), 7(ii), 7(iii) and 7(iv).	of original shipping documents and BL/AWB. 3.Payment of 20% of the purchase value will be made after physical verification by a project mentoring committee. Since bidders are allowed to quote in INR or USD , we request you to modify clause V, as clause 4 to be read as incase of bidders who quotes in US$, letter of credit (LC) will be opened and payment would be released as per payment milestones.	
16			Please provide the specification for the software suite item mentioned at Sl no 6 as per the schedule of requirement page no 20 ans also confirm if the software required is Processor based for 100 users or on Per node/system basis for 100 users	Please see the revised specifications in Annexure II
17	Page 19, Point 1, 2, 3, 4, 7, 8, 9, 10, 11, 12, 13 & 14		The specifications are not genric since it is from single OEM.	Please see the revised specifications in Annexure II
18	Page 19, Point 5 & 6		The specifications are not genric since it is from single OEM.	Please see the revised specifications in Annexure II
19	Page 19, Item No 15 & 16		The specifications are not genric since it is from single OEM.	Please see the revised specifications in Annexure II
20	Page 19, Point 6	Software suite to accompany the FPGA boards, for high level design, verification and implementation of VLSI designs	Please confirm if the Software required is Processor based or on Per Node basis.	Please see the revised specifications in Annexure II
21	Page 19, Point 1	Block Memory (MB) : 4 or more	FPGA board -2 block memory cannot be in MB for this particular size board as it is offered in KB (Kbits). We therefore request you to kindly change it to be read as Block memory (Kbits): Minimum 4k or more.	Please see the revised specifications in Annexure II
22	Page 19, Point 1	SDRAM (MB): 128 or more	In computer science terminology everything is binary. ie., it is either 0 or 1.	Please see the revised specifications in Annexure II

			Two values. So everything comes out to be a power of 2. The megabyte was designed thinking about the SI unit convention as power of 10. Like 1 MB is 106. But MiB was designed for power of 2. 1Mib is 2 power 20. Instead of power of 10. Therefore memory type mentioned is incorrect. Please change it to SDRAM)ie, Mib Mebibyte : 128 or more.	
23	Page 20, Point 6	Software suite to accompany the FPGA boards, for high level design, verification and implementation of VLSI designs	It is not clear if the license is required per user / node base or processor based. Kindly clarify.	Please see the revised specifications in Annexure II
24	Page 19, Point 1	FPGA boards – Type 1 FPGA specs: Logic elements/cells: 32,000 or more Block memory (kb): 1,800 or more Multipliers/DSP slices: 90 or more PLLs: 4 or more Board specs: SDRAM (Mb): 8 or more Flash (Mb): 32 or more Clock: 100 MHz oscillator I/O interfaces/Connectors: USB HID, USB-UART bridge, VGA	https://store.digilentinc.com/basys-3-artix-7-fpga-trainer-board-recommended-for-introductory-users/	Please see the revised specifications in Annexure II
25	Page 19, Point 2	FPGA boards – Type 2 FPGA specs: Logic elements/cells: 15,000 or more Block memory (Mb): 4 or more Multipliers/DSP slices: 240 or more PLLs: 5 or more Board specs: SDRAM (Mb): 128 or more Flash (Mb): 128 or more Clock: 100 MHz oscillator I/O interfaces/Connectors: Ethernet, USB HID, USB-UART bridge, VGA Other: Accelerometer, audio output, microphone, temperature sensor Displays: Two or more 7-segment	https://store.digilentinc.com/nexys-4-ddr-artix-7-fpga-trainer-board-recommended-for-ece-curriculum/	Please see the revised specifications in Annexure II

26	Page 19, Point 3	FPGA board with an on board processor FPGA specs: Logic elements/cells: 13,000 or more Block memory (kb): 500 or more Multipliers/DSP slices: 200 or more PLLs: 4 or more Board specs: Onboard processor: ARM Cortex A9 or equivalent SDRAM (Mb): 512 or more Flash (Mb): 256 or more Clock: 33 MHz and 100 MHz oscillator I/O interfaces/Connectors: Ethernet, LPC FMC, HDMI output, SD card, USB, USB-UART bridge, VGA Other: Audio, headphone, microphone connectors Display: OLED 25	https://store.digilentinc.com/zedboard-zyng-7000-arm-7-fpga-soc-development-board/	Please see the revised specifications in Annexure II
27	Page 19, Point 4	FPGA boards – 4 FPGA specs: Logic elements/cells: 200,000 or more Block memory (Mb): 12 or more Multipliers/DSP slices: 700 or more PLLs: 8 or more Board specs: SDRAM (Mb): 512 or more Flash (Mb): 128 or more Clock: 100 MHz oscillator I/O interfaces/Connectors: Ethernet, HDMI source and sink, MicroSD card, USB HID, USB-UART bridge Other: Audio codec Displays: OLED	https://store.digilentinc.com/genesys-2-kintex-7-fpga-development-board/	Please see the revised specifications in Annexure II
28	Page 20, Point 5	Advanced Development/Connectivity FPGA kit FPGA specs: Logic elements/cells: 650,000 or more Block memory (Mb): 50 or more Multipliers/DSP slices: 3500 or more Board specs: SDRAM (Gb): 8 or more Flash (Mb): 32 or more Clock: Two 200 MHz or more, one each for FPGA and memory. Programmably oscillator I/O interfaces/Connectors:	https://store.digilentinc.com/netfpga-sume-virtex-7-fpga-development-board/	Please see the revised specifications in Annexure II

		FMC HPC, PCI express (8-lane), SFP/SFP+ cages (4), USB-UART		
29	Page 20, Point 6	Software suite to accompany the FPGA boards, for high level design, verification and implementation of VLSI designs		Please see the revised specifications in Annexure II
30	Page 20, Point 7	DC motor driver interface board Drive a DC motor with operating voltage up to 12V Separate header for external motor feedback 2A H-bridge circuit PCB size: 1.2 in × 0.8 in	https://store.digilentinc.com/pmod-hb3-h-bridge-driver-with-feedback-inputs/	Please see the revised specifications in Annexure II
31	Page 20, Point 8	Thermometer/thermostat interface board Programmable over and under-temperature control pins 16-bit ambient temperature sensor. Typical accuracy better than 0.25ºC. No calibration required. 240 ms continuous conversion time	https://store.digilentinc.com/pmod-tmp2-temperature-sensor/	Please see the revised specifications in Annexure II
32	Page 20, Point 9	Digital to Analog Converter (DAC) board Two 8-bit DACs Four D/A conversion channels Maximum conversion rate of 1.875 MSa/s	https://store.digilentinc.com/pmod-da1-four-8-bit-d-a-outputs/	Please see the revised specifications in Annexure II
33	Page 20, Point 10	Keypad interface 16 momentary push-buttons Can detect simultaneous button presses Isolated rows and columns	https://store.digilentinc.com/pmod-kypd-16-button-keypad/	Please see the revised specifications in Annexure II
34	Page 20, Point 11	7-segment interfacing Two-digit high brightness seven-segment display Easily view a counter or timer Common Cathode configuration	https://store.digilentinc.com/pmod-ssd-seven-segment-display/	Please see the revised specifications in Annexure II
35	Page 20, Point 12	Analog to Digital Converter (ADC) board Two channel, 12-bit analog-to-digital converter Simultaneous A/D conversion at up to one MSa/s per channel Two 2-pole Sallen-Key anti-alias filters PCB size: 0.95 in × 0.8	https://store.digilentinc.com/pmod-ad1-two-12-bit-a-d-inputs/	Please see the revised specifications in Annexure II
36	Page 20, Point 13	LCD display 16×2 character LCD with parallel interface 192 predefined	https://store.digilentinc.com/pmodclp-character-lcd-with-parallel-interface/	Please see the revised specifications in Annexure II

		characters including 93 ASCII characters Up to 8 user-definable characters Read and write capability to and from the display		
37	Page 20, Point 14	Stepper motor driver For 4 and 6-pin motors Can drive both motors simultaneously Multiple LEDs to indicate signal propagation Jumper for optional external power	https://store.digilentinc.com/pmod-step-stepper-motor-driver/	Please see the revised specifications in Annexure II
38	Page 21, Point 15	VLSI Design front-end CAD tools suite: Circuit simulation, layout and verification • Schematic capture, netlisting, simulation setup and results viewing • Physical layout • Editing, schematic-driven layout, and top-level floorplanning and routing • High-performance circuit simulation for analog and RF circuits that provides: o Accurate, fast device noise analysis in time and frequency domains o Single-run Transient, DC, AC sensitivity analyses o Multi-tone Harmonic Balance & Shooting analyses o Device model libraries to include leading MOS, bipolar and MESFET transistor models such as BSIM3v3.x, BSIM4.3, EKV, Philips MM9 & MM11, SPv32, HiSIM, Mextram, VBIC, and HICUM o Real-time Design Tuning o Optimization o Post-processing o Power consumption analysis o Circuit and models profiling o Comprehensive waveforms viewing & analysis o Results browsing, sorting & filtering o Monte Carlo analysis o Incremental, dynamically controlled convergence o Monte Carlo acceleration using accuracy controlled metamodels o Native Multi-threading, Distributed Processing o		Please see the revised specifications in Annexure II

		Customizable aging models for aging, statistical aging and aging sensitivity simulations o Single-kernel Electro-thermal analysis solving full electrothermal system to accurately predict self-heating and thermal coupling o Advanced user-defined static and dynamic SOA checks o Analog and mixed-signal defect coverage, measuring likelihood-weighted test coverage of defects • RF specific circuit simulation capabilities: o Full-chip RF IC verification for wireless applications o Seamless integration with other IC design flows o Closed-loop phase noise analysis for PLLs and frequency synthesizers o Multi-tone steady-state analysis o Modulated steady-state analysis with RF/baseband partitioning o Built-in optimization capability • Physical verification tool: o Common verification for analog, digital and mixed-signal flows o Full support for VHDL, Verilog, SystemVerilog, VHDLAMS, Verilog-A/MS, SystemC o Unified coverage-driven mixed-signal verification o Enable top-down design and bottom-up verification of multi-million gate circuits o Physical verification for flat and hierarchical algorithms o Transistor-level, gate-level and hierarchical parameter extraction and back annotation		
39	Page 21, Point 16	EDA suite for HDL synthesis, design, verification of ASICs and FPGAs HDL design environment: o Create, analyze and manage complex FPGA and ASIC designs in VHDL,		Please see the revised specifications in Annexure II

		Verilog and System Verilog o Design checking rules and rulesets o Interactive HDL visualization and creation o Debug and analysis features o Concurrent design entry and checking o Efficient creation of RTL designs using text, tables, and graphics FPGA synthesis tool: o Support for Altera, Lattice, Microsemi and Xilinx o Vendor independent FPGA debug and validation o Fully automatic, partition-based, incremental synthesis o Integrated with incremental place-and-route o Automated exploration of synthesis implementation options o Control options for frequency, area and runtime o Mixed language support with SystemVerilog o ASIC prototyping support Verification tool: o Code coverage and analysis tools: Statement, expression, condition, FSM, etc. o Easy to use GUI o Support for Verilog, VHDL and SystemVerilog SoC verification tool		
40			Installation and training for FPGA boards (by certified trainers)	
41			Installation and training for CAD tools (by certified trainers)	

ANNEXURE II

Revised Schedule of Requirements

Sl No	Tender Specifications	Quantity
1	FPGA boards – 1 FPGA specs: Logic elements/cells: 32,000 or more Block memory (kb): 1,800 or more Multipliers/DSP slices: 90 or more PLLs: 4 or more Board specs: SDRAM (Mb): 8 or more I/O interfaces/Connectors: USB, VGA	100
2	FPGA boards – 2 FPGA specs: Logic elements/cells: 15,000 or more Block memory (Mb): 1.5 or more Multipliers/DSP slices: 100 or more PLLs: 4 or more Board specs: SDRAM (Mb): 64 or more I/O interfaces/Connectors: USB, VGA Other: Accelerometer, audio output, microphone, temperature sensor Displays: Two or more 7-segment	50
3	FPGA board with an onboard processor FPGA specs: Logic elements/cells: 13,000 or more Block memory (kb): 500 or more Multipliers/DSP slices: 200 or more PLLs: 4 or more Board specs: Onboard processor: ARM Cortex A9 or equivalent SDRAM (Mb): 64 or more I/O interfaces/Connectors: Ethernet, SD card, USB, USB-UART bridge, VGA Other: Audio, headphone, microphone connectors Display: OLED or Seven Segment	25

4	FPGA boards – 4 <u>FPGA specs</u>: Logic elements/cells: 100,000 or more Block or embedded memory (Mb): 5 or more Multipliers/DSP slices: 200 or more PLLs: 6 or more <u>Board specs</u>: SDRAM (Mb): 64 or more Clock: 50 MHz or more oscillator I/O interfaces/Connectors: Ethernet, MicroSD card, USB HID, USB-UART bridge Other: Audio codec Displays: OLED or LCD	10
5	Advanced Development/Connectivity FPGA kit <u>FPGA specs</u>: Logic elements/cells: 650,000 or more Block memory (Mb): 50 or more Multipliers/DSP slices: 3500 or more <u>Board specs</u>: SDRAM/DDR3 (Gb): 8 or more Flash (Mb): 32 or more Programmable oscillator I/O interfaces/Connectors: FMC HPC, PCI express, SFP/SFP+ cages (4)	10
6	Software suite to accompany the FPGA boards, for high level design, verification and implementation of VLSI designs	100 users
7	Motor interface board • Drive a DC motor with operating voltage up to 12V • Header for external motor feedback	25
8	Temperature interface board • 12 or more bit ambient temperature sensor. • Typical accuracy better than 1ºC. • No calibration required.	25
9	Digital to Analog Converter (DAC) board • Two 8-bit DACs	25
10	Keypad interface • 16 momentary push-buttons • Can detect simultaneous button presses • Isolated rows and columns	25
11	7-segment interfacing	25

	• Two-digit high brightness seven-segment display • Easily view a counter or timer • Common Cathode configuration	
12	Analog to Digital Converter (ADC) board • Two channel, 12-bit analog-to-digital converter • Simultaneous A/D conversion at up to one MSa/s per channel • Two 2-pole Sallen-Key anti-alias filters	25
13	Display board • 16×2 character LCD with parallel interface • 192 predefined characters including 93 ASCII characters • Up to 8 user-definable characters • Read and write capability to and from the display	25
14	VLSI Design front-end CAD tools suite: Circuit simulation, layout and verification • Schematic capture, netlisting, simulation setup and results viewing • Physical layout • Editing, schematic-driven layout, and top-level floorplanning and routing • High-performance circuit simulation for analog and RF circuits that provides: o Accurate, fast device noise analysis in time and frequency domains o Single-run Transient, DC, AC sensitivity analyses o Device model libraries to include leading MOS, bipolar and MESFET transistor models o Real-time Design Tuning o Optimization o Post-processing o Power consumption analysis o Circuit and models profiling o Comprehensive waveforms viewing & analysis o Results browsing, sorting & filtering o Monte Carlo analysis o Incremental, dynamically controlled convergence o Monte Carlo acceleration using accuracy controlled meta-models o Native Multi-threading, Distributed Processing o Single-kernel Electro-thermal analysis solving full electro-thermal system to accurately predict self-heating and thermal coupling • RF specific circuit simulation capabilities: o Closed-loop phase noise analysis for PLLs and frequency synthesizers o Multi-tone steady-state analysis o Built-in optimization capability • Physical verification tool: o Common verification for analog, digital and mixed-signal flows	50 users

	○ Full support for Verilog ○ Unified coverage-driven mixed-signal verification ○ Enable top-down design and bottom-up verification of multi-million gate circuits ○ Physical verification for flat and hierarchical algorithms ○ Transistor-level, gate-level and hierarchical parameter extraction and back annotation	
15	EDA suite for HDL synthesis, design, verification • HDL design environment: ○ Create, analyze and manage complex designs in VHDL, Verilog and System Verilog ○ Design checking rules and rulesets ○ Interactive HDL visualization and creation ○ Debug and analysis features ○ Concurrent design entry and checking ○ Efficient creation of RTL designs using text, tables, and graphics • FPGA synthesis tool: ○ Support for Altera, Lattice, Microsemi and Xilinx ○ Vendor independent FPGA debug and validation ○ Fully automatic, partition-based, incremental synthesis ○ Integrated with incremental place-and-route ○ Automated exploration of synthesis implementation options ○ Control options for frequency, area and runtime • Verification tool: ○ Easy to use GUI ○ Support for Verilog, VHDL SoC verification tool	50 users