Fault Injection Framework to Study Soft Error Resilience on FPGA

Jhalak Sharma[1], Dr. Otmane Ait Mohamed[2], Dr. Nanditha Rao[3]
1-IIIT-Bangalore (India) 2-ConcordiaUniversity, Montreal (Canada) 3-IIIT-Bangalore (India)

GOAL:

To design a controller-based fault injection framework for RISC-V core, program it on FPGA and to study the probability of multiple bit-flips.

INTRODUCTION:

- Soft errors are random, non-recurring change of register states due to energetic particles interacting with silicon.
- As technology node scales down, the radiation particles with lesser energies could induce a soft error in adjacently places gates/transistor.
- Reduced voltage and shrinking node capacitance makes the devices more susceptible to soft errors.
- Significant impact on Circuit reliability.

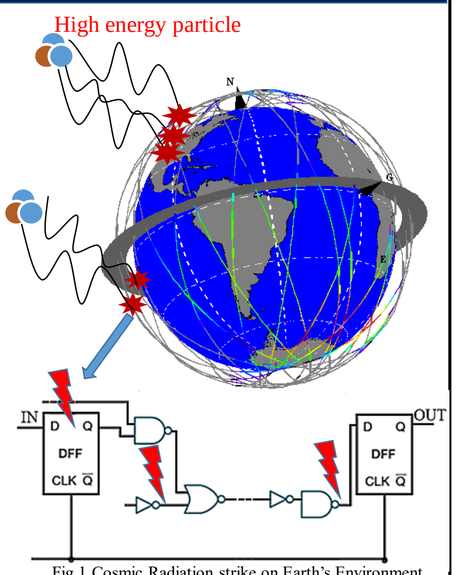


Fig.1 Cosmic Radiation strike on Earth's Environment
Fig.2 Radiation sticking electronic gate/transistors
Source: TI Radiation Handbook for Electronics

Why FPGA?

- Re-configurable feature unlike ASICs
- Re-programmable inflight/remotely
- Permit to integrate several digital functional units in one FPGA
- Radiation effects are challenging due to:
  - Device features are now comparable to radiation interaction characteristics
  - Space environment knowledge
  - Rapid evolution of technology

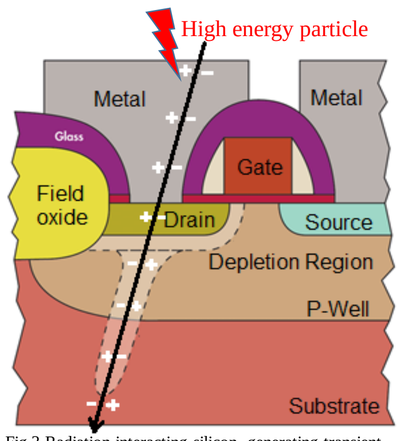
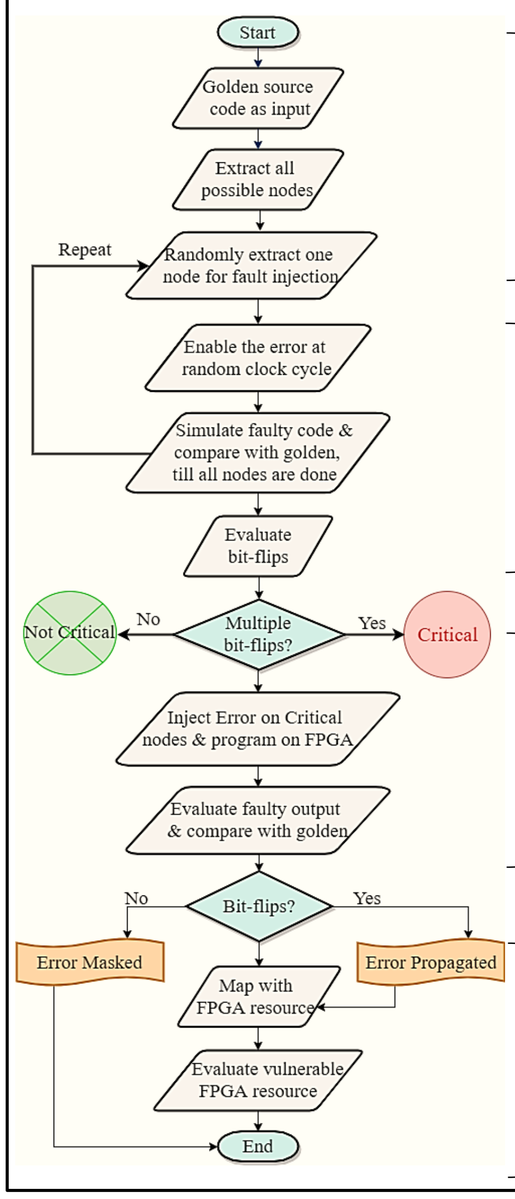


Fig.3 Radiation interacting silicon, generating transient
Source: CERN

METHODOLOGY:



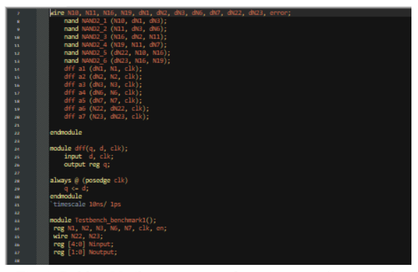
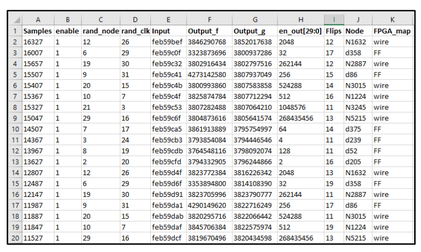


Fig.4 Golden Verilog source code as input to framework



Samples	enable	rand_node	rand_clk	Input	Output_f	Output_g	en_out[29:0]	Flips	Node	FPGA_map
16327	1	12	26	feb59bef	3846290768	3852017638	2048	12	N1632	wire
16007	1	6	29	feb59c0f	3323873696	3800937286	32	17	d358	FF
15657	1	19	30	feb59c32	3802916434	3802797516	262144	12	N2887	wire
15507	1	9	31	feb59c41	4273142580	3807937049	256	15	d86	FF
15407	1	20	15	feb59c4b	3800993860	3807583858	524288	14	N3015	wire
15367	1	10	7	feb59c4f	3825874784	3807712294	512	16	N1224	wire
15327	1	21	3	feb59c53	3807282488	3807064210	1048576	11	N3245	wire
15047	1	29	16	feb59c6f	3804873616	3805641574	268435456	13	N5215	wire
14507	1	7	17	feb59ca5	3861913889	3795754997	64	14	d375	FF
14367	1	3	24	feb59cb3	3793854084	3794446546	4	11	d239	FF
13967	1	8	19	feb59cdb	3764548116	3798092074	128	11	d52	FF
13627	1	2	20	feb59cfd	3794332905	3796244866	2	16	d205	FF
12807	1	12	26	feb59d4f	3823772384	3816226342	2048	13	N1632	wire
12487	1	6	29	feb59d6f	3353894800	3814108390	32	19	d358	FF
12147	1	19	30	feb59d91	3823705996	3823790777	262144	11	N2887	wire
11987	1	9	31	feb59da1	4290149620	3822716249	256	17	d86	FF
11887	1	20	15	feb59dab	3820295716	3822066442	524288	11	N3015	wire
11847	1	10	7	feb59daf	3845706384	3822575974	512	19	N1224	wire
11527	1	29	16	feb59dcf	3819670496	3820434598	268435456	13	N5215	wire

Fig.5 Error injection & critical node extraction in Python

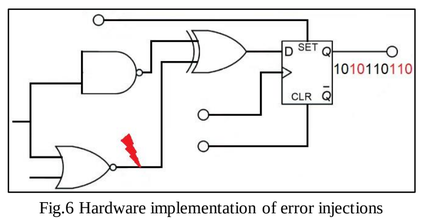


Fig.6 Hardware implementation of error injections

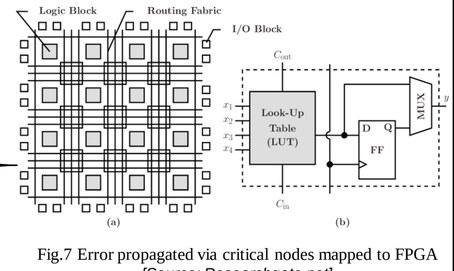


Fig.7 Error propagated via critical nodes mapped to FPGA
[Source: Researchgate.net]

RESULTS:

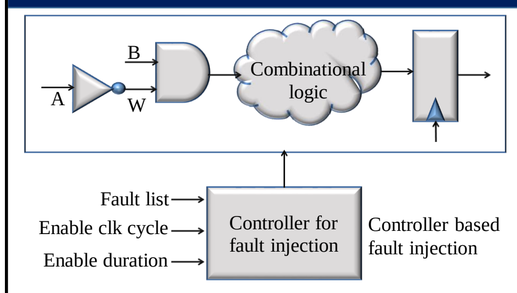


Fig 8. Fault injection Framework

Experimental Setup:

- Source code – Verilog
- FPGA implementation – Xilinx Vivado
- FPGA Board – Digilent Basys3 Artix-7
- Technology node – 28nm
- Scripting/Automation – Python

Observations:

Fig. 9 Synthesized Netlist with error injected (c6288)
Blue- LUT, Red – Flip-flops

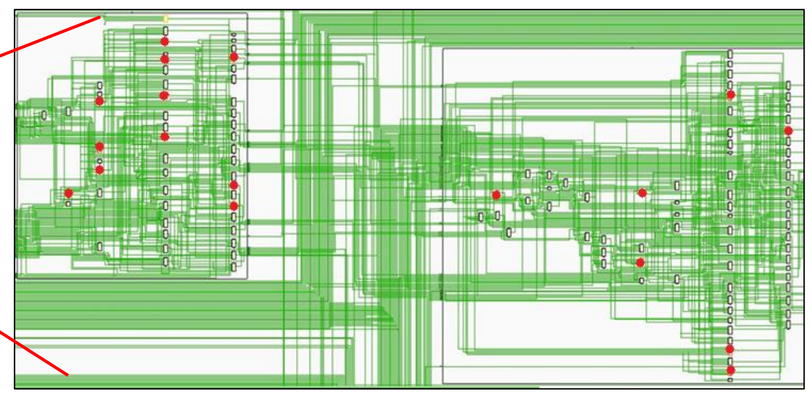


Fig. 10 Highlighted spots are critical nodes which cause multiple output flips

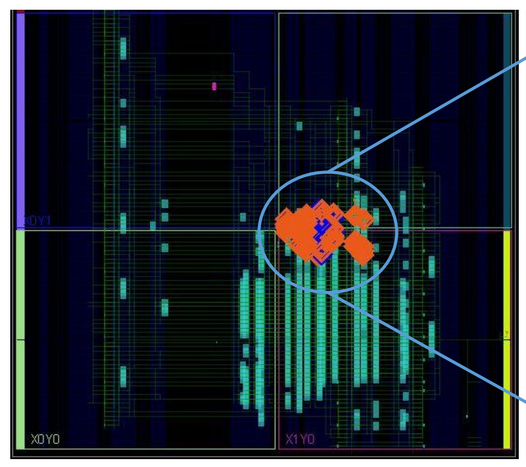


Fig. 11 FPGA Layout of the circuit with error injected (c6288)
Blue- LUT, Red – Flip-flops

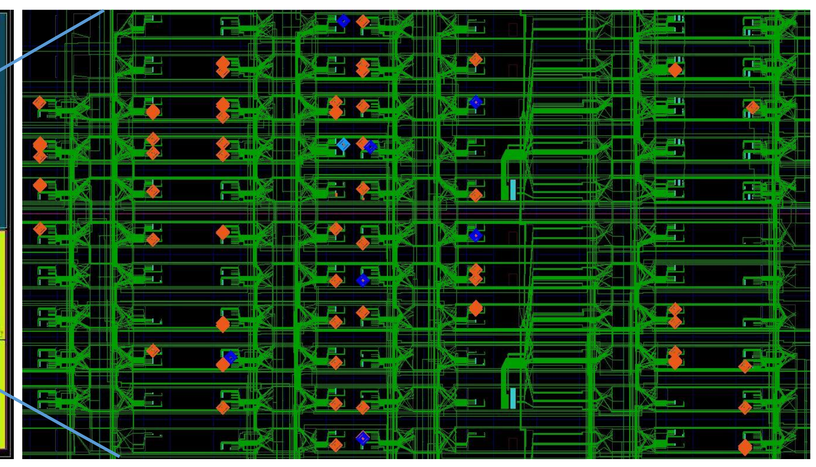


Fig. 12 Highlighted spots are vulnerable FPGA resources.

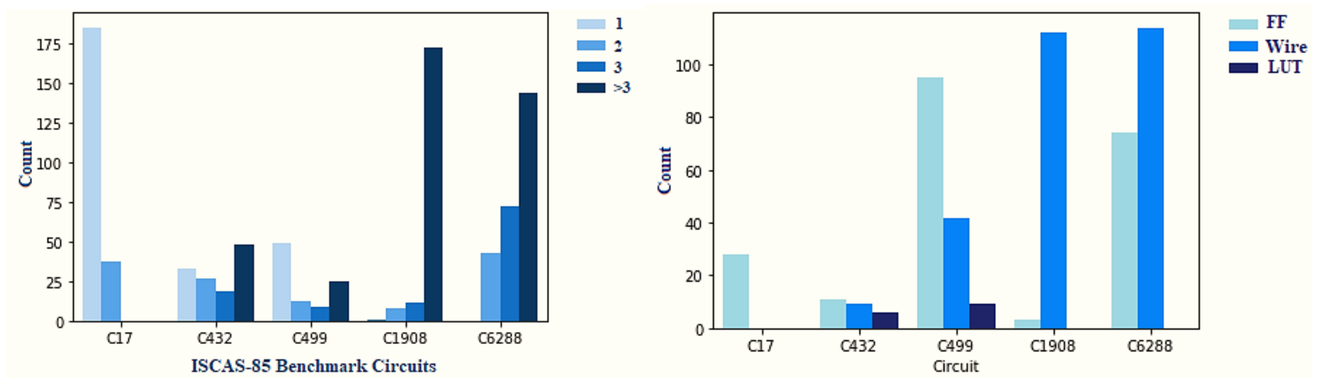


Fig. 13 Single and Multiple Bit-flips Statistics for ISCAS-85 benchmarks with flip-flops added to input and output nodes
Fig. 14 Vulnerable FPGA resources corresponding to multiple bit upsets

Conclusions:

- Number of multiple flips (>2) is substantial in most circuits
- Memory element (flip-flops) and the interconnects are the most vulnerable component on the FPGA, which can corrupt multiple outputs.
- Single radiation interaction with silicon can propagate to multiple gates/transistor.

REFERENCES:

1. ABDUL RAFAY KHATRI, M. M. (n.d.). Instrumentation Technique for FPGA based Fault Injection Tool. *Recent Advances in Financial Planning and Product Development*.
2. Ghazanfar Asadi, M. B. (2005). Soft Error Rate Estimation and Mitigation for SRAM Based FPGAs. *FPGA'05, February 20–22, 2005, Monterey, California, USA.*, (p. 12).
3. Haissam Ziade1, R. A. (2011). A New Fault Injection Approach to Study the Impact of Bitflips in the Configuration of SRAM-Based FPGAs. *The International Arab Journal of Information Technology*.
4. https://www.microsemi.com/product-directory/reliability/4883-see

CONTACT INFO: 1. jhalak.sharma@iiitb.org (IIIT-Bangalore , India) 2. ait@ece.concordia.ca (Concordia University, Montreal, Canada) 3. nanditha.rao@iiitb.ac.in (IIIT-Bangalore, India)